Fabrication of SOI substrates with ultra-thin Si layers

K.D. Hobart, F.J. Kub, G.G. Jernigan, M.E. Twigg and P.E. Thompson

A simple technique for the fabrication of ultra-thin silicon-on-insulator (SOI) substrates is presented. The bond-and-etch-back technique utilising an Si_xGe_{1-x} etch stop has been combined with the thin film separation by hydrogen implantation approach, and SOI substrates with ultra-thin (< 5nm) Si layers have been successfully fabricated.

Ultra-thin (≤ 10nm) silicon-on-insulator (SOI) substrates are desirable for many technologies including extreme scaling of MOS transistors [1, 2], dual-gate MOSFETs [3], quantum wires and dots [4], and compliant or universal substrates [5 – 7]. In the past, ultra-thin semiconductor layers have been produced by successive oxidation and oxide etching of SOI wafers [4] and, in the case of GaAs, by epitaxial lift-off [8] and etch stop [6] techniques.

In this Letter, an approach is reported which combines two existing SOI substrate fabrication techniques and effectively eliminates the primary disadvantage of each method. The bond-and-etch-back technique for fabricating SOI substrates (BESOI) has been combined with the hydrogen implantation and separation technique (also called smart-cut) [9]. The BESOI process has been shown to produce highly uniform thin (~ 200nm) Si layers by incorporating an epitaxial Si_xGe_{1-x} etch stop layer into the sacrificial host substrate prior to wafer bonding [10, 11]. The disadvantage of the BESOI approach is that the entire host substrate must be removed by a laborious sequence of grinding, polishing, and etching. In addition, overall thickness uniformity during the substrate thinning process must be critically maintained since the etch selectivity of Si over SiGe is limited (≤ 100). The H-implantation and separation process also utilises wafer bonding, but in this case a heavy dose of implanted H, together with subsequent annealing, produces H-exfoliation that releases the host substrate to generate the SOI structure. Following exfoliation, the surface has a microroughness of ~ 8nm [9] and must be given a slight chemomechanical polish to produce a smooth surface. This step degrades the Si layer thickness uniformity and makes the process unsuitable for producing very thin Si films. The process presented here avoids the above disadvantages and, as shown below, is a simple method for producing uniform SOI wafers with Si thicknesses of < 10nm.

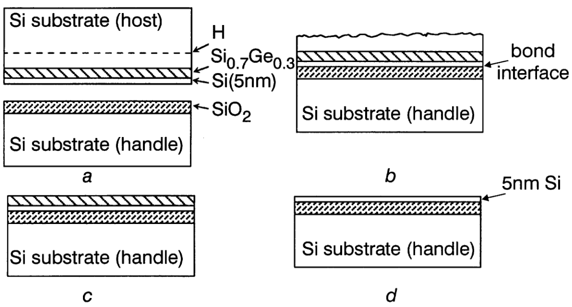

Fig. 1 *Ultra-thin SOI fabrication process*

a Preparation of handle and host wafers prior to bonding
b Bonded wafer pair shown after separation of host substrate
c SOI structure prior to removing SiGe etch stop
d Ultra-thin SOI after removal of SiGe etch stop

The process sequence is shown in Fig. 1. 100mm diameter, 10 Ωcm, *n*-type, (100) orientation substrates were thermally oxidised in dry 0_2 to produce 120nm of SiO_2 for 'handle' wafer fabrication. On similar starting substrates, Si and Si_xGe_{1-x} films were epitaxially grown to form the 'host' substrates. The nominal layer specifications were a 20nm Si buffer, followed by 30nm of $Si_{0.7}Ge_{0.3}$ and 4nm of Si. All layers were B-doped to ~ $10^{15}cm^{-3}$. The host substrates were implanted at room temperature with H_2^+, with an ion energy of 180keV and a dose of $4.5 \times 10^{16}cm^{-2}$ (see Fig. 1*a*). Handle and host substrates were rendered hydrophilic by $NH_4OH:H_2O_2:H_2O$::1:1:4 and $HCl:H_2O_2H_2O$::1:1:4 cleaning procedures. After a final rinse in de-ionised water, the wafers were spun dry. Wafer bonding was performed in a class 100 laminar flow bench using a custom designed jig to align the major wafer flats. Infrared transmission imaging showed the existence of several macrovoids near the wafer edge; otherwise the bonded pair was void-free. The wafer pair was annealed at 250°C for 4h to improve the bond strength. To separate the host substrate from the etch stop layer and handle wafer, the wafer pair was heated to 550°C for 10min in N_2 (Fig. 1*b*). Separation of the host substrate left ~800nm of Si (including the SiGe etch stop and Si capping layer) on the SiO_2 film with a mean surface roughness of ~5–7nm, as measured by stylus profilometry. Film separation was successful over the entire 100mm wafer. Nomarski microscopy revealed a textured surface resulting from the exfoliation process. Aqueous KOH (10% by weight) was then used to etch the Si and stop at the SiGe (Fig. 1*c*). The etch rate for Si at room temperature was found to be ~30nm/min and the etch selectivity to $Si_{0.7}Ge_{0.3}$ was found to be ~20. Following the Si etch, Nomarski microscopy revealed no detectable surface roughness. The films were specular and extremely uniform to the eye. Since the etch rate of SiO_2 was negligible in KOH, the remaining film thickness was measurable by stylus profilometry across the macrovoids near the wafer edge. The film thickness (Si + SiGe) was found to be 36nm. X-ray photoelectron spectroscopy (XPS) indicated that the actual etch stop composition was closer to $Si_{0.68}Ge_{0.32}$. The SiGe layer was then selectively removed in a solution of $HF:H_2O_2:CH_3COOH$::1:2:3 [12]. The etch rate of $Si_{0.7}Ge_{0.3}$ was found to be ~100nm/min at room temperature and the etch selectivity to Si was nearly 1000. Examination by Nomarski microscopy revealed no detectable surface features and the film appeared to be specular and uniform to the eye.

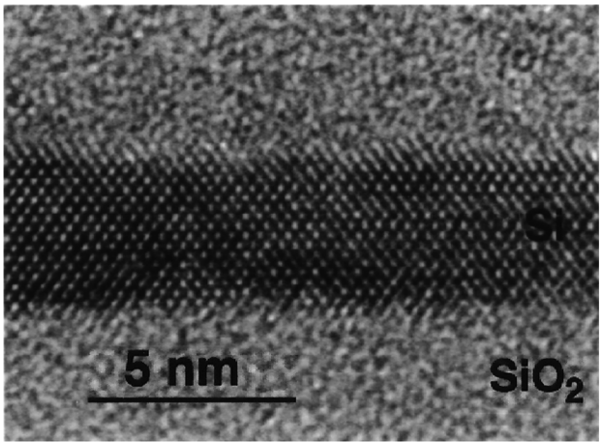

Fig. 2 *High resolution cross-sectional transmission electron micrograph of ultra-thin (~4nm) silicon layer of SOI wafer*

The ultra-thin SOI films were further characterised by XPS and high-resolution cross-sectional transmission electron microscopy (HRXTEM). The Si film thickness was estimated with XPS by measuring the attenuation of Si 2p core level electrons from the buried SiO_2. This peak is unambiguously identified since the binding energy is chemically shifted by +4.5eV with respect to Si 2p electrons in bulk Si. From the known inelastic mean free path of Si 2p electrons in Si (2.1nm [13]) and the measured attenuation of the signal (92.4%), the Si thickness was estimated to be 5.0±0.5nm. Ge 2p electrons were also detected with an intensity equivalent to that produced by a 5.0nm thick $Si_{0.98}Ge_{0.02}$ alloy with uniform Ge concentration. The actual Ge profile was not determined. HRXTEM was performed on the as-fabricated ultra-thin SOI structure. A micrograph is shown in Fig. 2. From TEM it was determined that the Si thickness was closer to 4.0nm and was uniform to within 20% over the sample studied.

In conclusion, ultra-thin Si (< 5nm) SOI has been fabricated, for the first time, by combining the BESOI and film separation by H-implantation techniques. This combined approach effectively eliminates the drawbacks associated with the individual processes and is capable of producing extremely thin SOI films with excellent thickness uniformity and low surface roughness. This approach should have numerous applications for microelectronics, quantum regime devices, and compliant substrates for lattice-mismatched heteroepitaxial growth.

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